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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,649	06/04/2001	Mitsuhiro Ono	P/3156-22	4262

7590 11/29/2005

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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2352 7590 09/23/2003

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4

Office Action Summary	Application No.	Applicant(s)	
	09/873,649	ONO, MITSUHIRO	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2001* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-7* is/are rejected.

7)☒ Claim(s) *1-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *3* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it has references to the drawings. The references to the drawings should be removed. Correction is required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: lines 11-12 on page 2 recite "external instruction RAM" when referring to external instruction ROM in Figure 4. The Examiner suggests changing "external instruction RAM" to external instruction ROM.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "said external instruction ROM" in lines 3 and 5. There is insufficient antecedent basis for this limitation in the claim. The Examiner would like to

point out that if "external instruction RAM" in line 6 of claim 1 were changed to external instruction ROM, the rejection would be withdrawn.

Claim 4 recites the limitation "said external instruction ROM" in lines 3 and 5. There is insufficient antecedent basis for this limitation in the claim.

Claims 5-7 depend from claim 3, hence inherit the deficiencies of claim 3.

Claim Objections

3. Claims 1-7 are objected to because of the following informalities: Claim 1 recites "external instruction RAM" in line 6, which is inconsistent with dependant claims that depend from claim 1 (see previous 112 rejections). The Examiner would like to point out that if "external instruction RAM" in line 6 of claim 1 were changed to external instruction ROM, the objection would be withdrawn.

Claims 2-7 depend from claim 1, hence inherit the deficiencies of claim 1.

Appropriate correction is required.

Allowable Subject Matter

4. Claims 1-7 would be allowable if the suggested corrections were implemented (see Claim Rejections - 35 USC § 112 and Claim Objections sections, above).

The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The present invention pertains to an integrated circuit for modem including an instruction RAM which is in plural bank configuration and functions as a cache memory for an external instruction ROM including a hardware unit for conducting an error correction processing, interleave processing and digital signal processing for transmission and reception data and a CPU which executes an instruction which is prefetched to the instruction RAM for controlling said hardware unit, wherein that said CPU and said hardware time-divisionally share part of the banks of said instruction RAM.

Claim 1 recites various features:

"a hardware unit for conducting an error correction processing, interleave processing and digital signal processing for transmission and reception data; an instruction RAM comprising a plurality of banks, which functions as a cache memory of an external instruction RAM; and a CPU which executes an instruction which is prefetched to the instruction RAM for controlling said hardware unit, wherein that said CPU and said hardware time-divisionally share part of the banks of said instruction RAM." [Emphasis Added]

The Prior Art of record teach a hardware unit for conducting an error correction processing (see ECC Logic 118 in Figure 4 in Matteson), interleave processing (col. 5, lines 41-43 in Matteson teach Figure 4 is a block diagram of an error correction code pipeline for interleaved memory systems) and digital signal processing for transmission and reception data (The Abstract in Matteson teaches a CPU for the purposes of processing and transferring digital data, hence Matteson teaches a digital signal

processing for transmission and reception data); an instruction RAM comprising a plurality of banks, which functions as a cache memory of an external instruction RAM (Fig. 2 of Matteson teaches Cache Memory for Coprocessor 52 is divided in to two banks Cache A 62A and Cache B 62B; col.1, line 68 of Matteson teaches that instructions are stored in the computer's memory 6, 10 and 12 of Figure 1a; and col. 2, lines 32-52 in Matteson teach that Cache memory is used to speed-up access of data from system memory).

The prior art however are not concerned with and do not teach that said CPU and said hardware time-divisionally share part of the banks of said instruction RAM as taught by claim 1. Hence the prior art taken alone or in any combination fail to teach the claimed novel feature in claim 1.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Burrer, Charlotte A. et al. (US 5172379 A) teaches memory systems, which use multiple banks of memory modules and a unique interleaved, pipelined technique for accessing said memory banks when performing read and write operations. Maeda, Takeshi et al. (US 5761695 A) teaches a control method and apparatus of a cache memory which can improve an accessing speed of the memory and control method and apparatus of a memory capable of interleave control in an information processing apparatus having a cache memory and a main memory and in an information processing apparatus having a memory capable of interleave control.

Matteson, Keith D. et al. (US 5335234 A.) teaches data pipelining for error correction/detection circuitry in computer systems using interleaved memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100